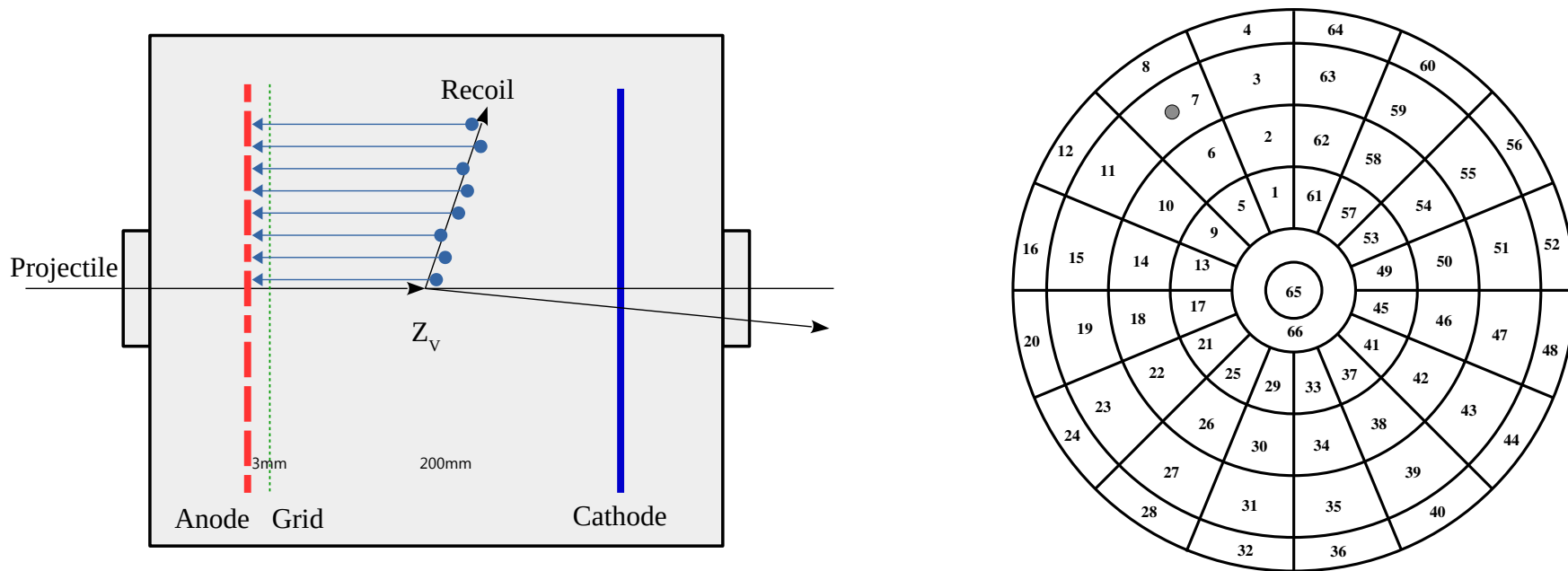


Investigation of the front end electronics for the proton radius experiments

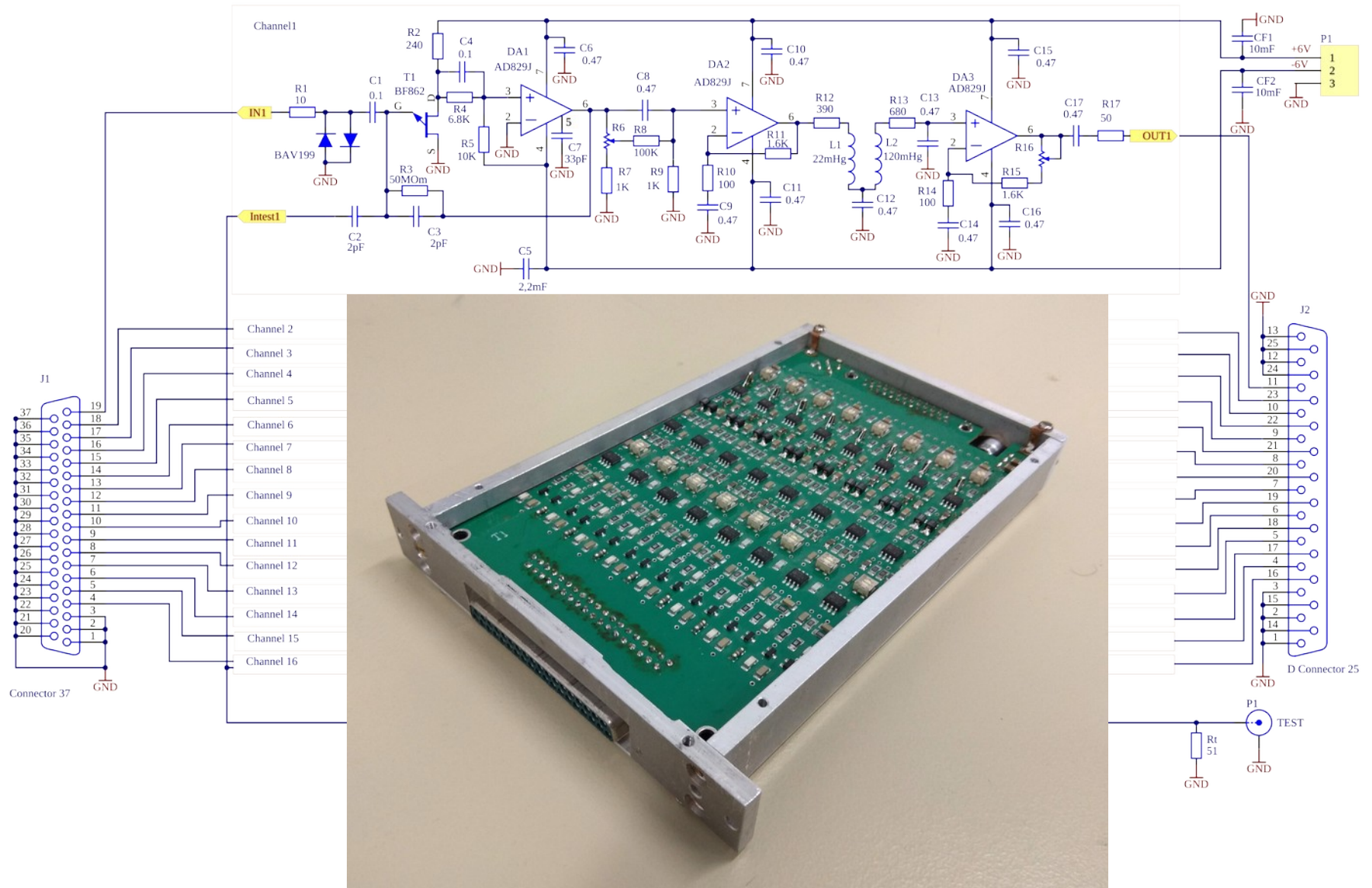
Alexander Inglessi • PNPI Gatchina
TPC Collaboration Meeting • 10 March 2020 • TU Mainz

TPC prototype

Active target: gas target + ionization chamber



Front-end prototype



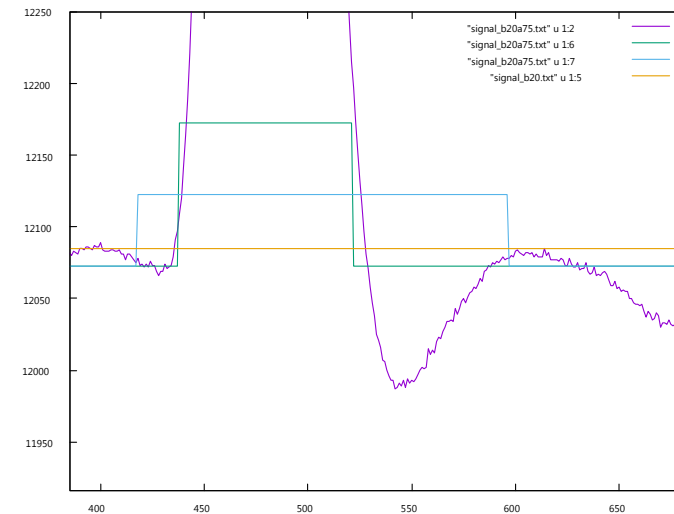
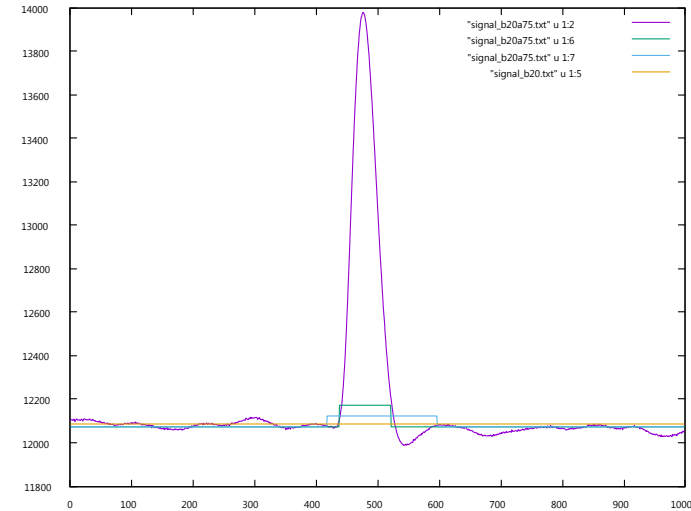
SIS3316 VME digitizers



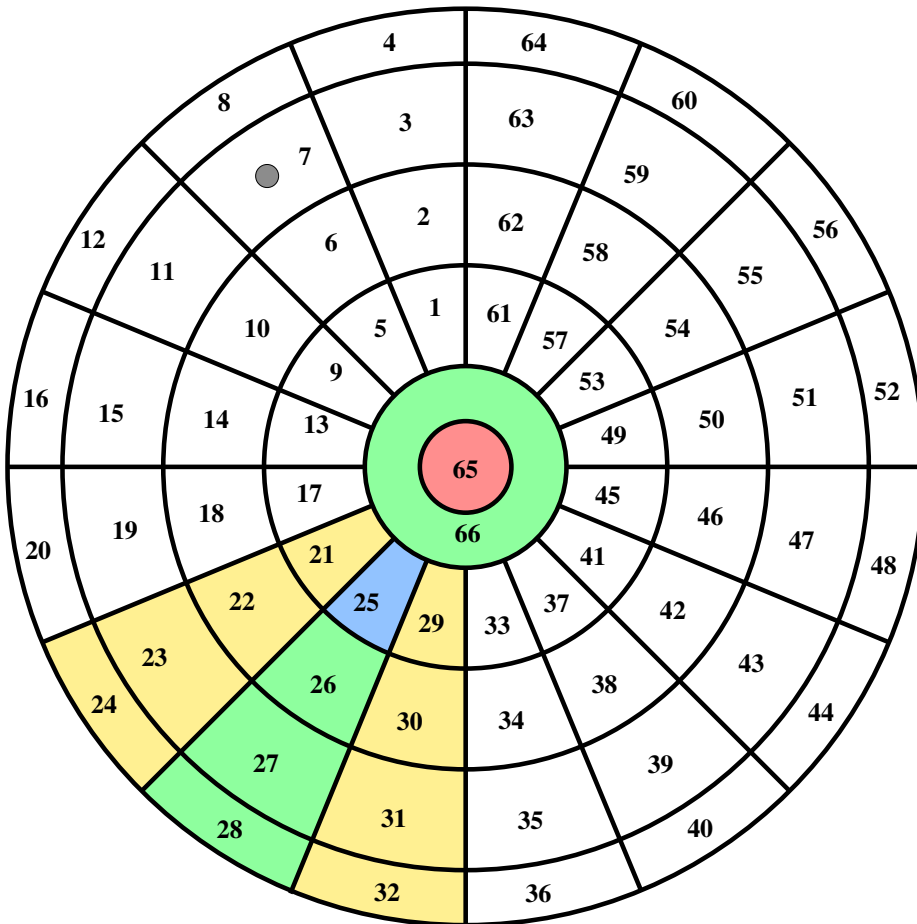
- 16 channels per module
- 25 MHz (40 ns bin),
up to 250 MHz
- 14 bit, 5 V (2 V) range
- Int./ext. trigger
- MAW energy/threshold

Individual signal analysis

- Signal smoothing
- Peak search
- Obtaining time parameters by slope differentiation
- Pedestal correction
- Peak raw signal integration \rightarrow energy

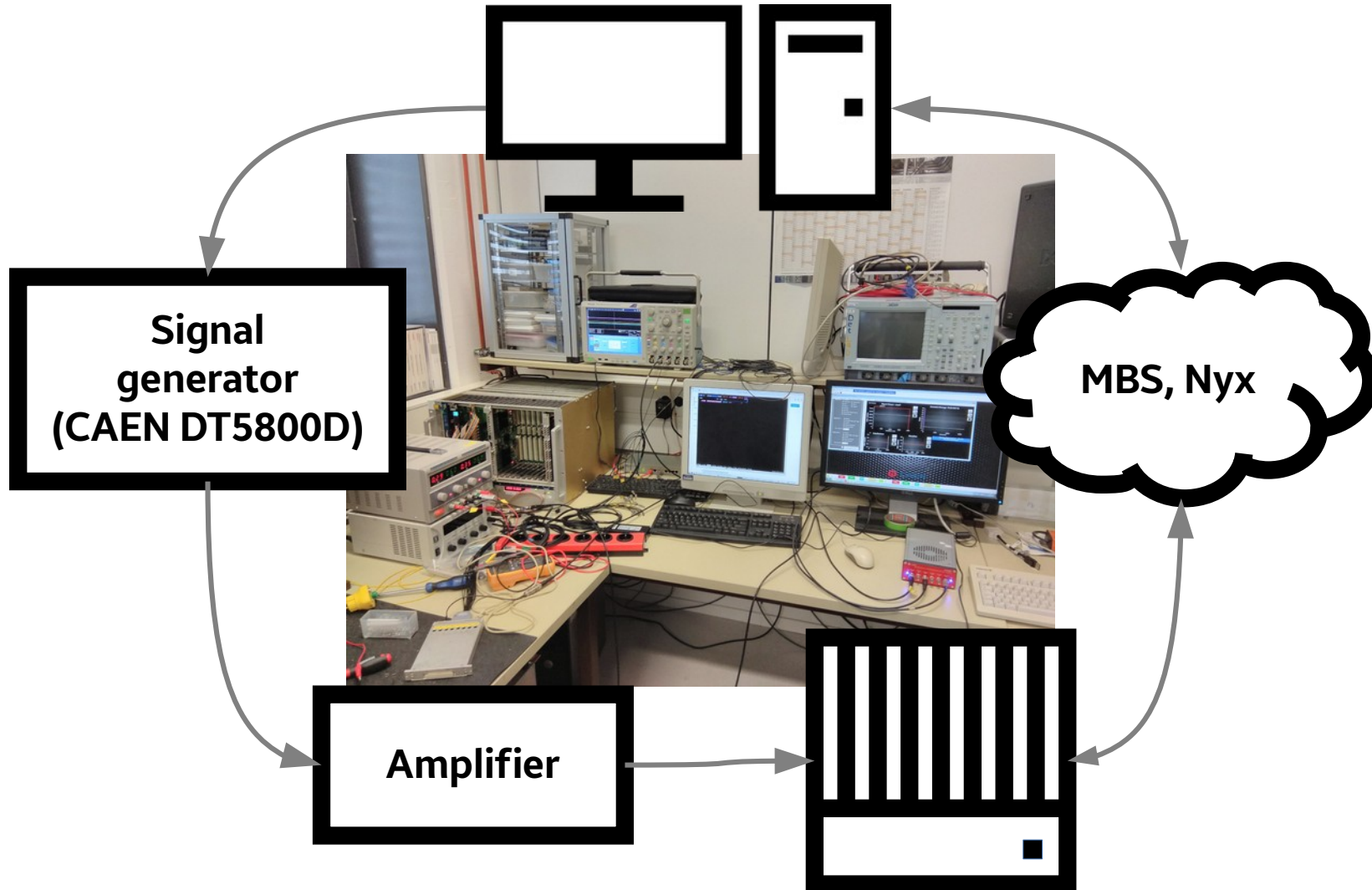


Recoil track search

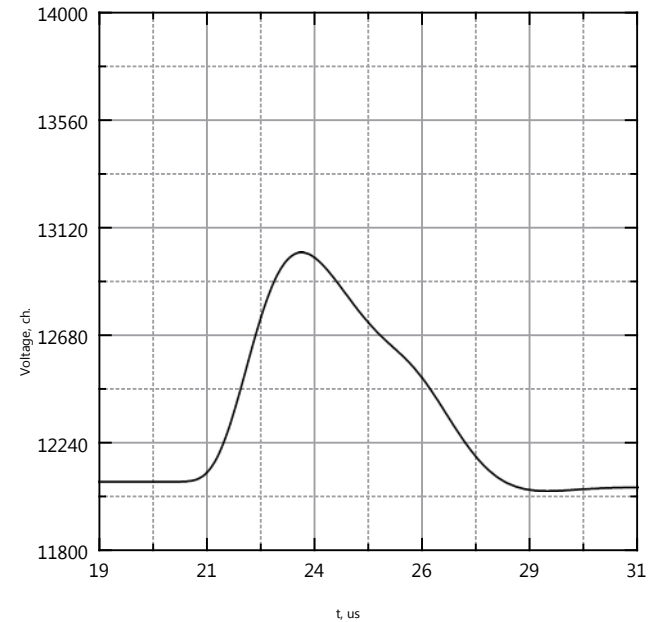
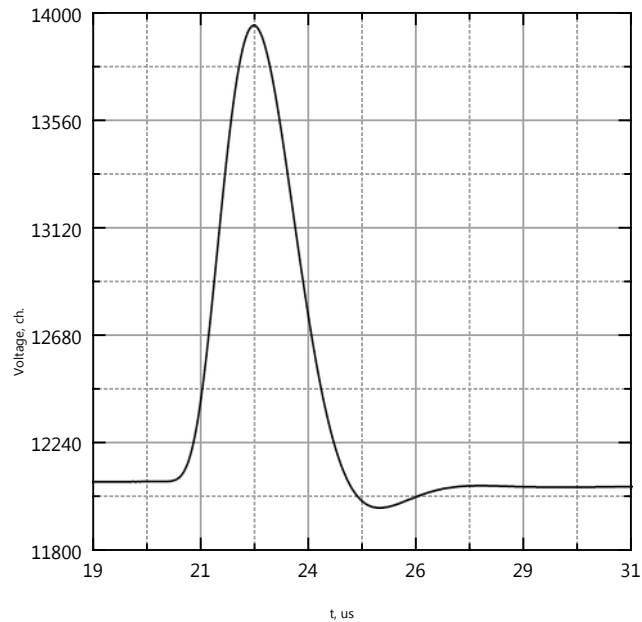
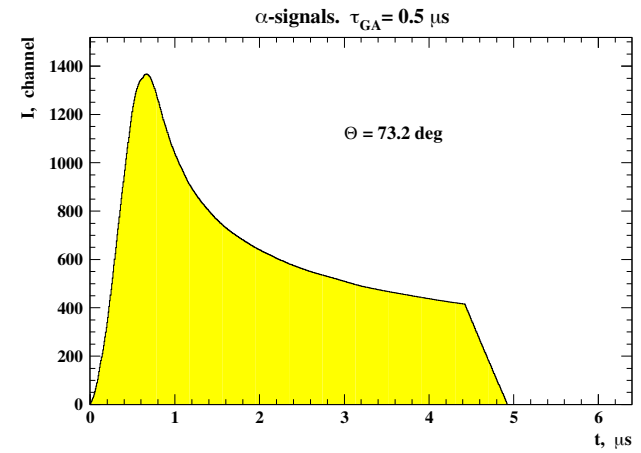
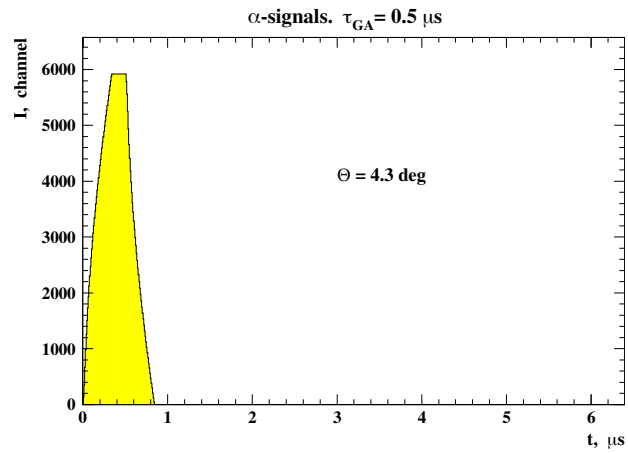


- Initial algorithm implementation
- Tested in beam experiments with different detector orientation

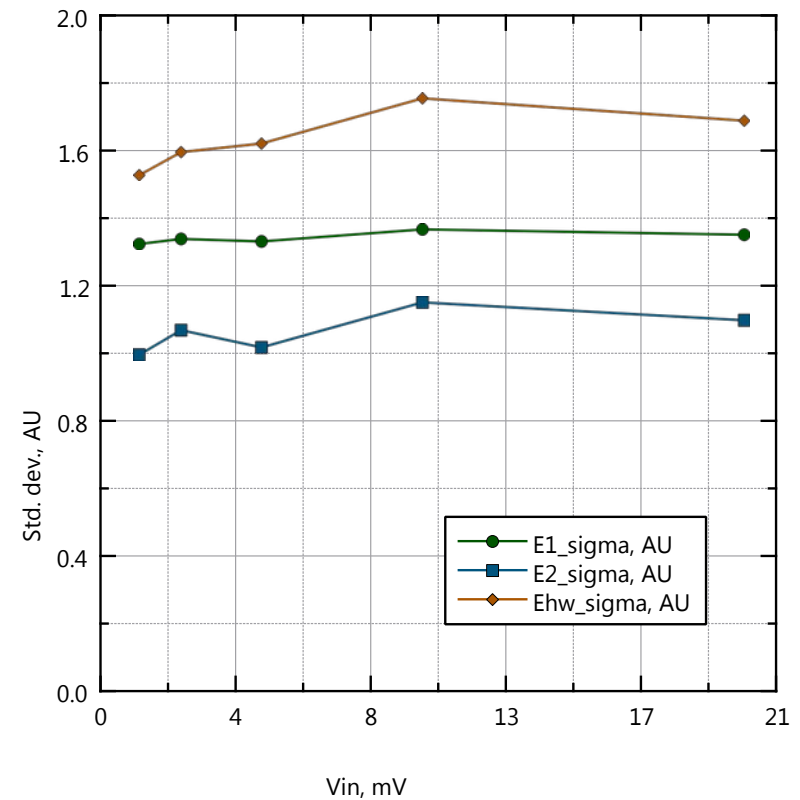
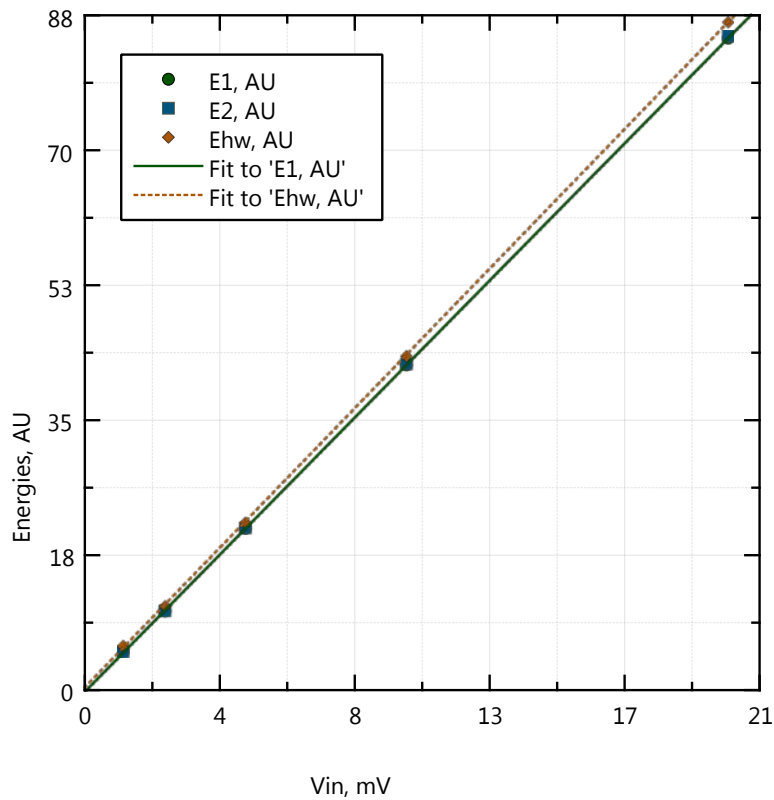
Test station at GSI



Generated amplifier input signals

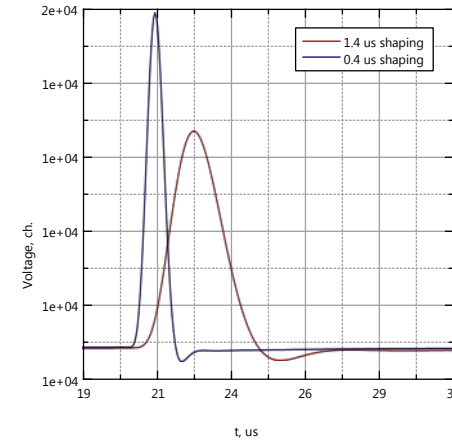
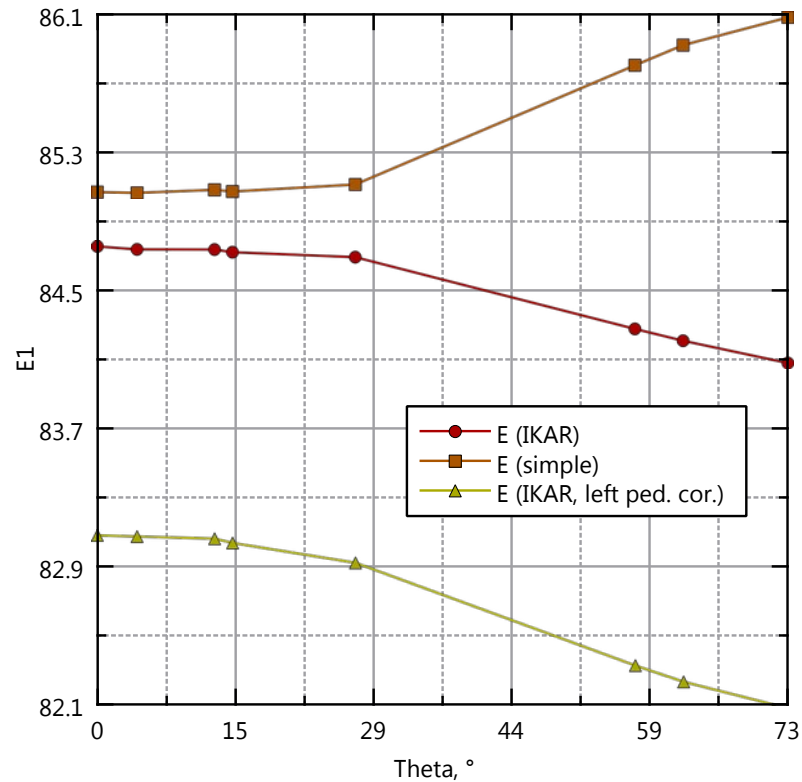


Results: energy vs. V_{in} (short signal)



1 AU \approx 27 keV

Results: integral vs. signal width



- Energy must be corrected
- Individual channel calibration required

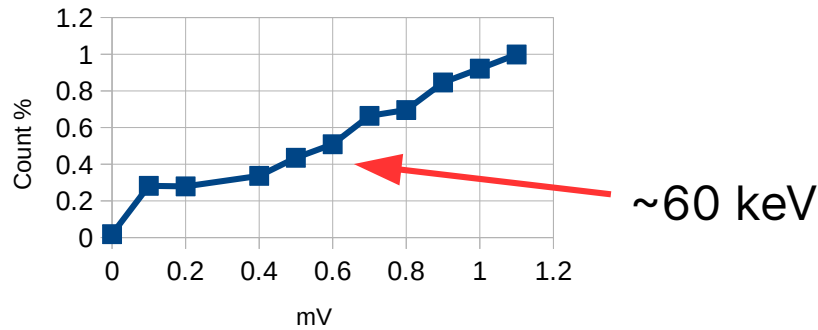
1 AU \approx 27 keV

Results: FADC trigger thresholds

1.4 μ s shaping

1.4 μ s, 60PT, 60GT

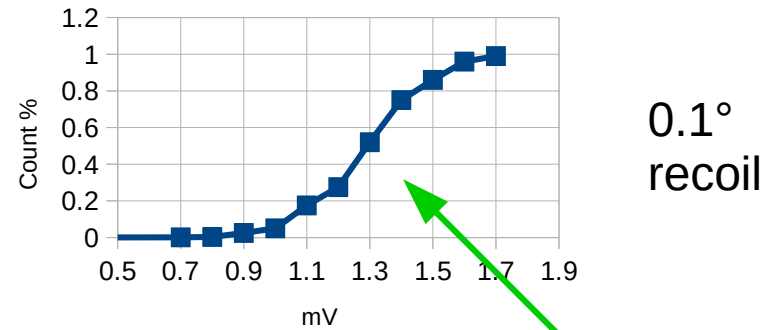
0.1° recoil, "2mv" threshold



0.4 μ s shaping

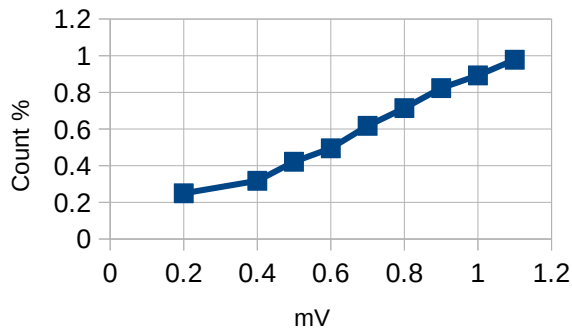
0.4 μ s, 60PT, 60GT

0.1° recoil, "2mv" threshold



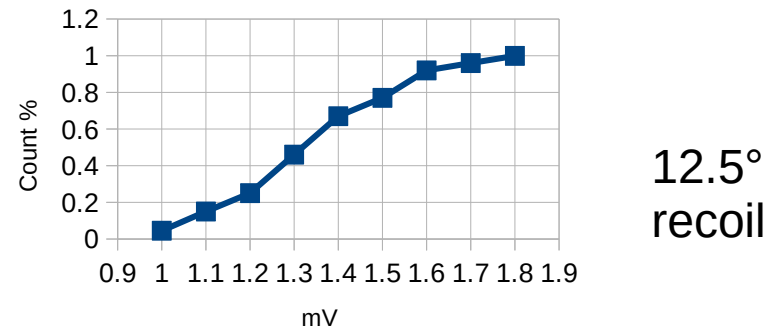
1.4 μ s, 60PT, 60GT

12.5° recoil, "2mv" threshold



0.4 μ s, 60PT, 60GT

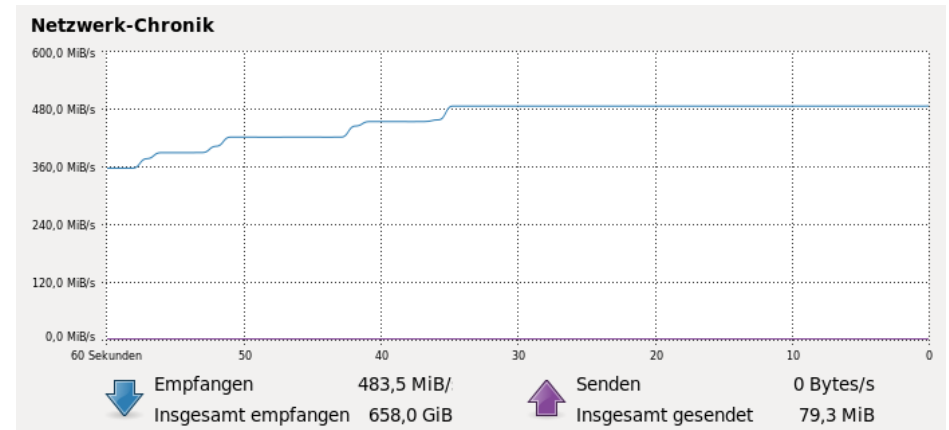
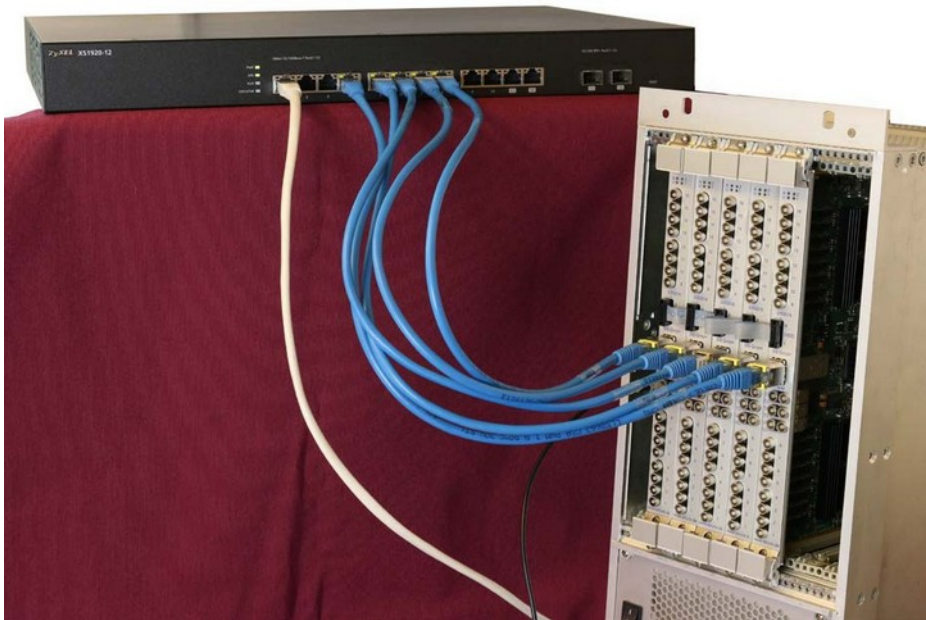
12.5° recoil, "2mv" threshold



Shaping time optimization

- time vs. energy resolution
- full integration vs. beam influence minimization
- smaller shaping for beam anode?

Fast FADC readout



- 5 FADCs with 1 Gbit/s Ethernet
- 10 Gbit/s PC link
- ~480 MB/s throughput achieved
- 20x faster than current setup

Conclusions

- High time and energy resolution requirements
- Energy must be corrected
- Thresholds may be lowered
- Time resolution studies with generator are in progress
- Algorithm optimization needed for smaller shaping time (noise filters, possibly higher sampling rate?)
- Goal: final front-end electronics recommendation this year

Thank you!

CAEN DT5800D Digital Detector Emulator



- 2 analog outputs
- 16 bit D/A converter
- 125 Msamples/s
- Constant/Poisson rate
- 4096 points to store waveforms
- White noise, 1/f noise emulation
- Random Walk (baseline drift)
- Interference generation
- USB, Windows control app

Moving average window

